IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| APPLICANT(S): | Masakatsu Nakai | ATTORNEY DOCKET NO.: | 09792909-5817 |
| SERIAL NO. | 10/806,902 | GROUP ART UNIT: | 2838 |
| DATE FILED: | March 23, 2004 | EXAMINER: | Matthew Van Nguyen |
| INVENTION: | "SEMICONDUCTOR CHIP" | | |

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

**AMENDMENT "B"**

S I R:

This Amendment "B" is filed in response to the non-final Office Action of March 29, 2006. Please reconsider the application in view of the amendment and remarks presented below.

IN THE CLAIMS

This listing of claims replaces all prior listings.

1. (canceled).

2. (currently amended) A semiconductor chip comprising: ~~as set forth in claim 1,~~

a delay monitoring means for finding a critical path delay characteristic of a target circuit subjected by power supply voltage control;

a voltage setting signal generating means for generating a voltage setting signal for setting a power supply voltage to be supplied to the target circuit based on the result of monitoring of delay by the delay monitoring means; and

a voltage setting restricting means for restricting the maximum value of the power supply voltage set in the voltage setting signal to a predetermined value,

wherein said voltage setting restricting means comprises:

a first storing means for storing a maximum voltage setting signal for setting the maximum value of the power supply voltage to be restricted, and

a comparing means for comparing the maximum value of the power supply voltage set by the maximum voltage setting signal stored in the first storing means with the value of the power supply voltage set by the voltage setting signal and outputting the signal having a lower voltage setting.

3. (original) A semiconductor chip as set forth in claim 2, wherein said first storing means is able to electrically erase and rewrite the stored signals.

4. (original) A semiconductor chip as set forth in claim 2, wherein said first storing means includes one or more fuse circuits and stores signals according to a conductive state or a nonconductive state of the fuse in the fuse circuits.

5. (original) A semiconductor chip as set forth in claim 3, further comprising:

a second storing means for storing a plurality of maximum voltage setting signals, and

a maximum voltage signal transferring means for reading out a maximum voltage setting signal selected in accordance with the signal indicating the operation state of the target

circuit from the second storing means and transferring the same to the first storing means.

6. (canceled).

7. (currently amended) A semiconductor chip comprising: ~~as set forth in claim 6,~~

a delay monitoring means for finding a critical path delay characteristic of a target circuit subjected by power supply voltage control;

a voltage setting signal generating means for generating a voltage setting signal for setting a power supply voltage to be supplied to the target circuit based on the result of monitoring of delay by the delay monitoring means; and

a voltage setting restricting means for restricting the maximum value of the power supply voltage set in the voltage setting signal to a predetermined value,

wherein said voltage setting restricting means determines the maximum value of the power supply voltage to be restricted in accordance with a signal indicating an operation state of the target circuit, and

wherein said voltage setting restricting means includes:

a plurality of first storing means for storing maximum voltage setting signals for setting the maximum value of the power supply voltage to be restricted;

a selecting means for selecting a maximum voltage setting signal corresponding to a signal indicating the operation state of the target circuit from among the maximum voltage setting signals stored in the plurality of first storing means; and

a comparing means for comparing the maximum value of the power supply voltage set by the maximum voltage setting signal selected by the selecting means with the value of the power supply voltage set by the voltage setting signal and outputting the signal having a lower voltage setting.

8. (original) A semiconductor chip as set forth in claim 7, wherein said first storing means is able to electrically erase and rewrite the stored signals.

9. (original) A semiconductor chip as set forth in claim 7, wherein said first storing means includes one or more fuse circuits and stores signals according to a conductive state or a nonconductive state of the fuse of the fuse circuits.

## REMARKS

Claims 1-9 are pending in the application. In the non-final Office Action of March 29, 2006, the Examiner made the following disposition:

A.) Rejected claims 1 and 6 under 35 U.S.C. 102(e) as allegedly being anticipated by *Seki '467*.

B.) Objected to claims 2-5 and 7-9.

Applicant addresses the Examiner's disposition below.

A.) Rejection of claims 1 and 6 under 35 U.S.C. 102(e) as allegedly being anticipated by *Seki '467*:

Claims 1 and 6 have been canceled without prejudice.

Applicant respectfully submits the rejection has been overcome and requests that it be withdrawn.

B.) Objection to claims 2-5 and 7-9:

Applicants respectfully acknowledge the Examiner's finding of allowable subject matter in claims 2-5 and 7-9.

Claim 2 has been amended to be placed into independent form including the subject matter of its base claim and any intervening claims. Therefore, claim 2, as amended, is allowable.

Claims 3-5 depend directly or indirectly from claim 2 and are therefore allowable for at least the same reasons that claim 2 is allowable.

Claim 7 has been amended to be placed into independent form including the subject matter of its base claim and any intervening claims. Therefore, claim 7, as amended, is allowable.

Claims 8 and 9 depend directly or indirectly from claim 7 and are therefore allowable for at least the same reasons that claim 7 is allowable.

Applicants respectfully submit the objection has been overcome and request that it be withdrawn.

## CONCLUSION

In view of the foregoing, it is submitted that claims 2-5 and 7-9 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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